Detection of Light

VII. IR Arrays & Readout

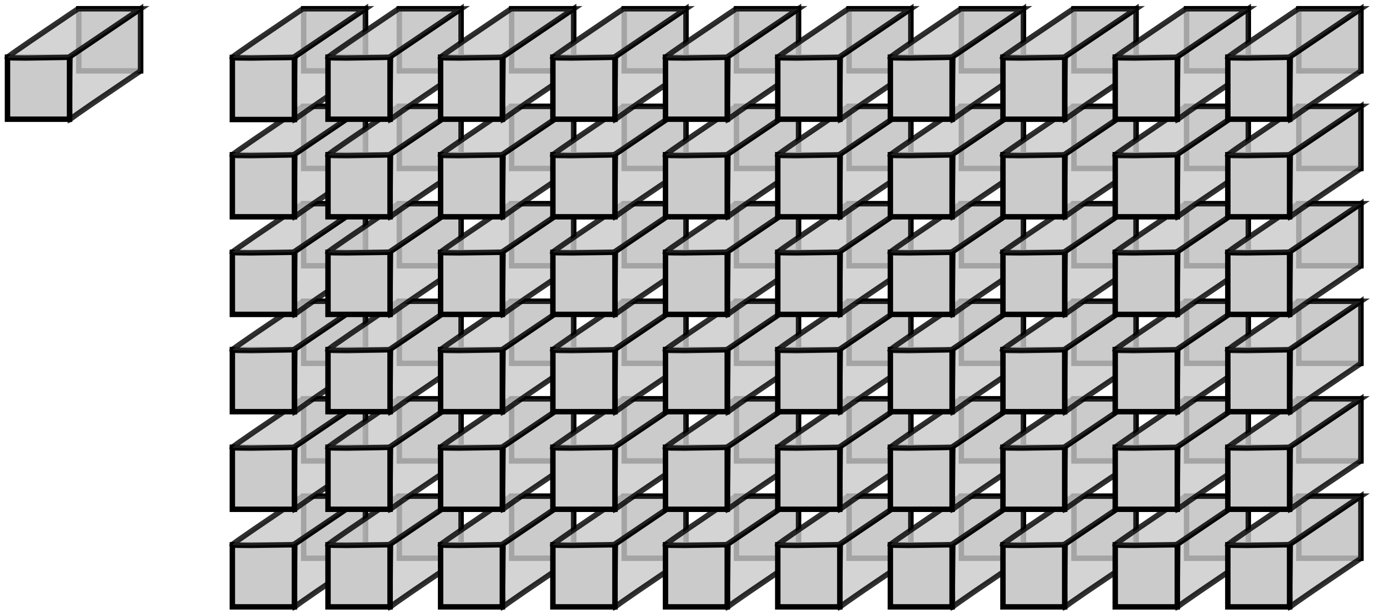
VIII.CCDs & Readout

This lecture course follows the textbook "Detection of Light" by George Rieke, Cambridge University Press

Detector Arrays

Detector Arrays

Arrays are formed from individual photoconductors:



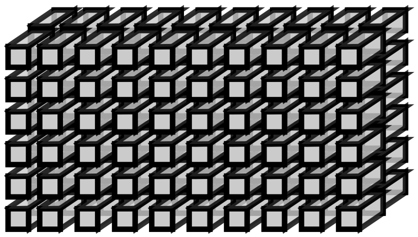
+ Readout Electronics

= Detector Array

Two Types of Detector Arrays
(a simplified comparison)

IR Arrays

$$(1\mu m - 40\mu m)$$

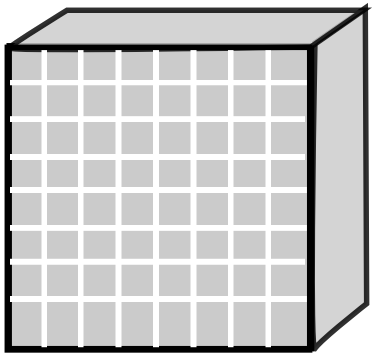


+ directly access individual pixels

- complex and expensive

Charge Coupled Devices (CCDs)

$$(0.1nm - 1\mu m)$$



+ monolithic structure integrated in Si wafer

- charge transfer inefficiencies

Infrared Arrays

Construction

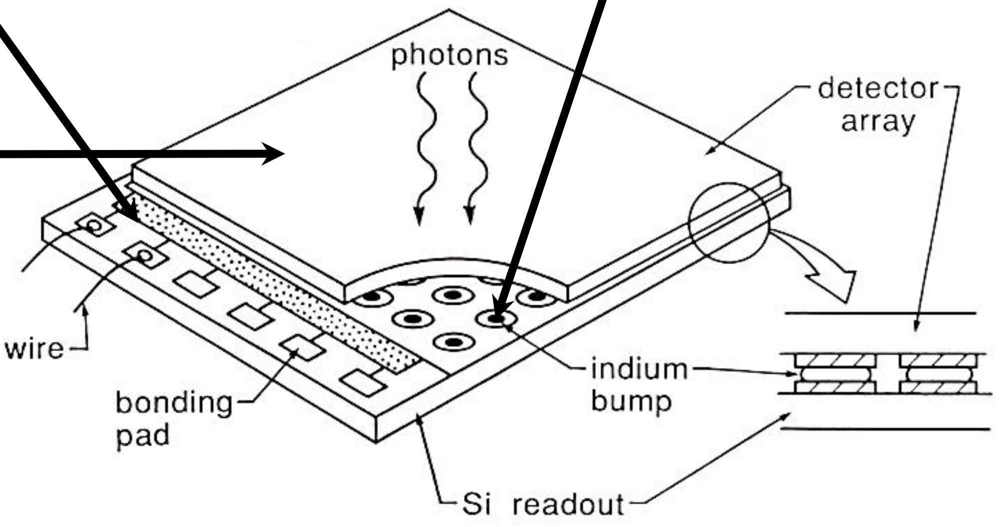
Construction of IR Arrays (1)

Make a grid of readout amplifiers in Silicon

Deposit Indium bumps on both sides

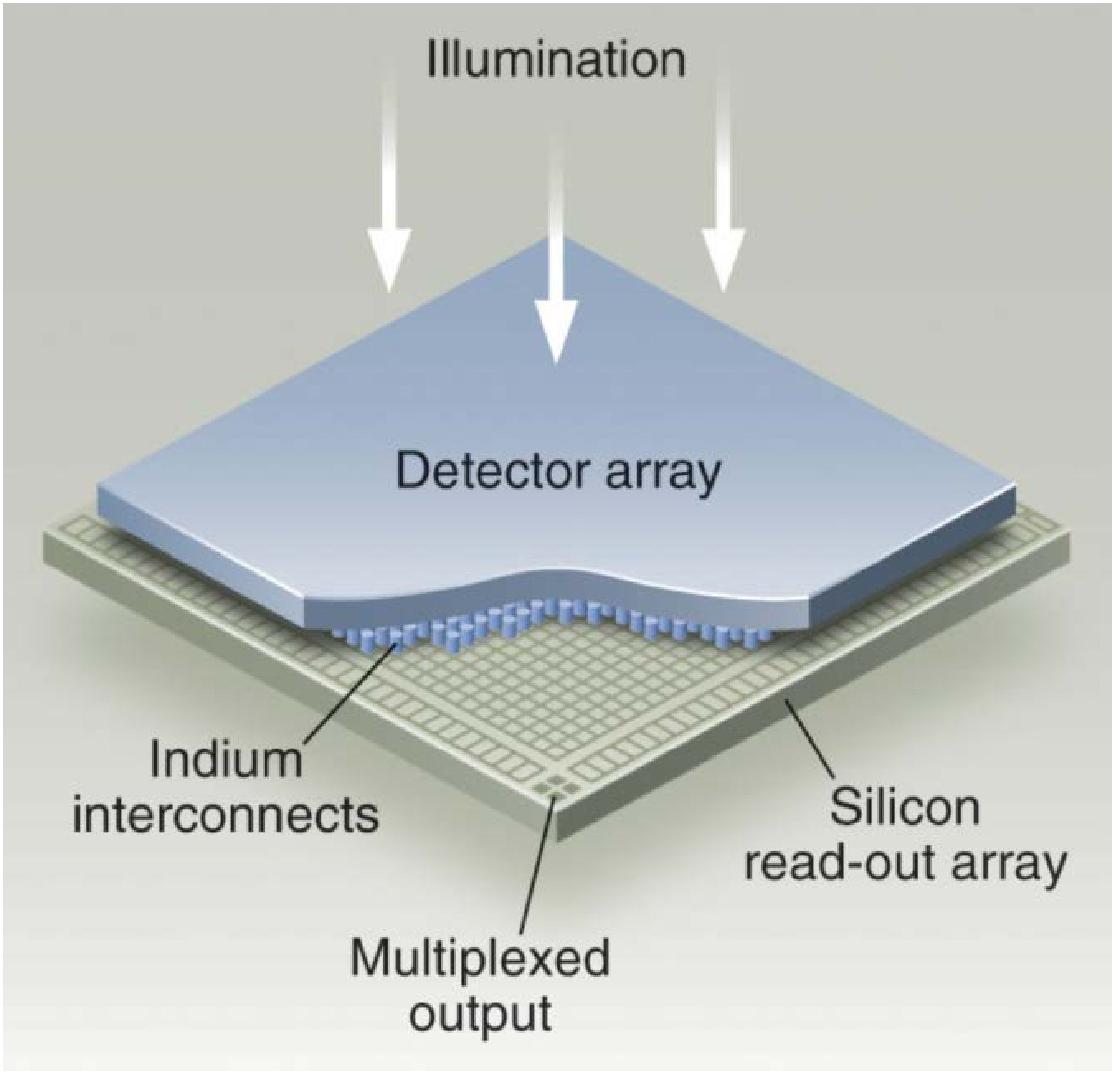
Make a matching image of detector pixels

Squeeze them together to make a hybrid array



Why Indium? It's a soft metal and will still be ductile at cryogenic temperatures!

Construction of IR Arrays (2)



Note that the actual pixel structure is given by the bonds and readouts, not the photoconductor.

Thermal Mismatch

Thermal mismatch can be a problem when cooling a hybrid array!

Consider the differential thermal contraction between photosensitive material and silicon readout wafer:

$$\alpha_{Si} \sim 2.6 \times 10^{-6}$$
$$\alpha_{HgCdTe} \sim 5 \times 10^{-6}$$

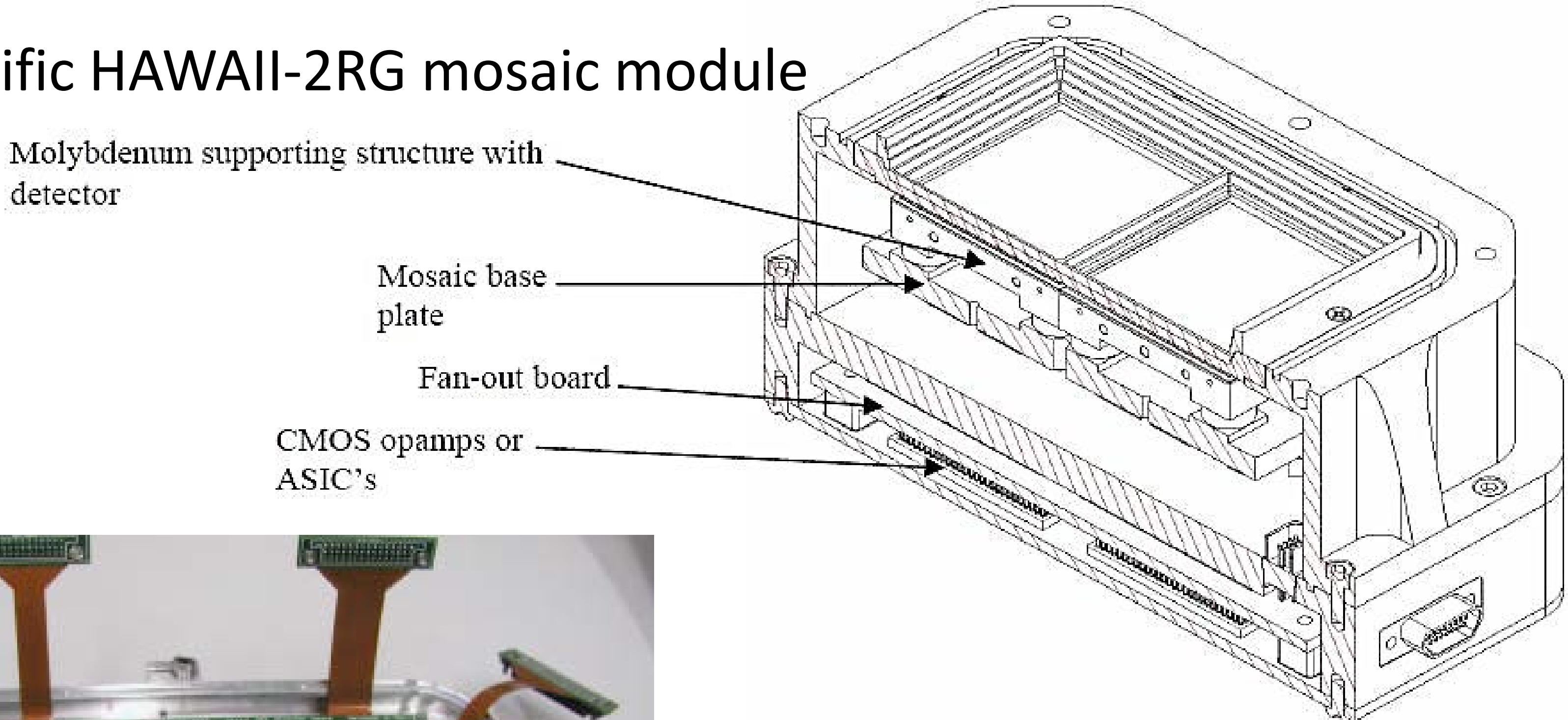
$$\frac{\Delta L}{L_0} = \alpha_L \Delta T$$

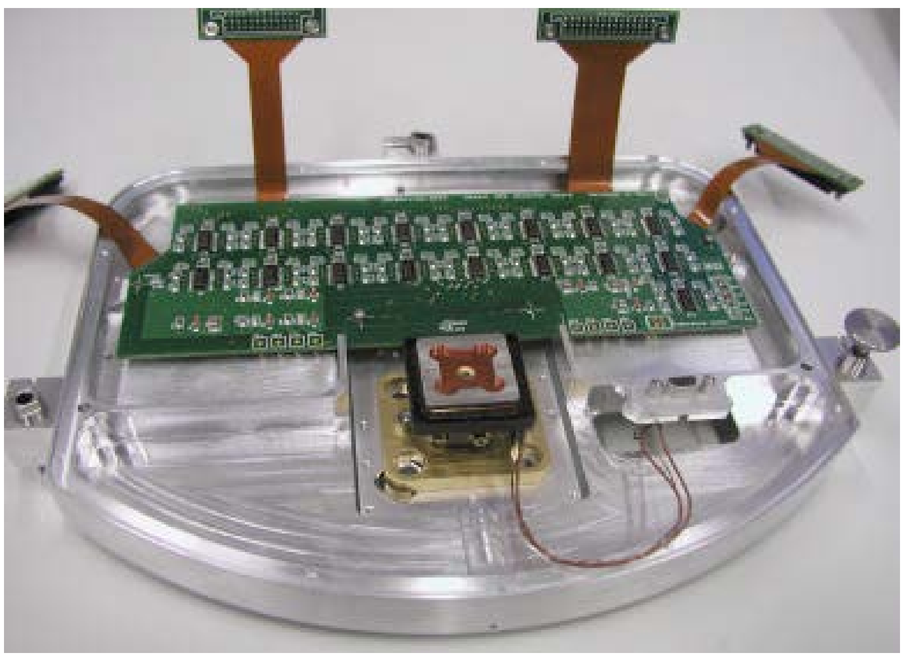
$$\Delta L_{mis} = L_0(\alpha_{HgCdTe} - \alpha_{Si})\Delta T = 36.9mm \times 2.4 \times 10^{-6} \times 200K = 17\mu m$$

...so, for a 2k × 2k array, we have a mismatch of about 1 pixel
The Indium bumps may break, and we get “dead pixels“.

Detector Mounts

GL Scientific HAWAII-2RG mosaic module





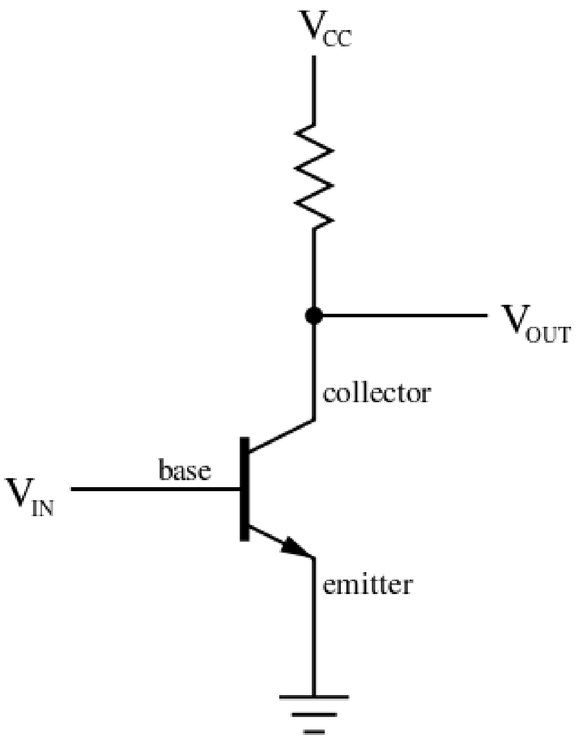
Detector mount for ESO's SPIFFI with cryogenic preamplifiers for 32 (+2) readout channels

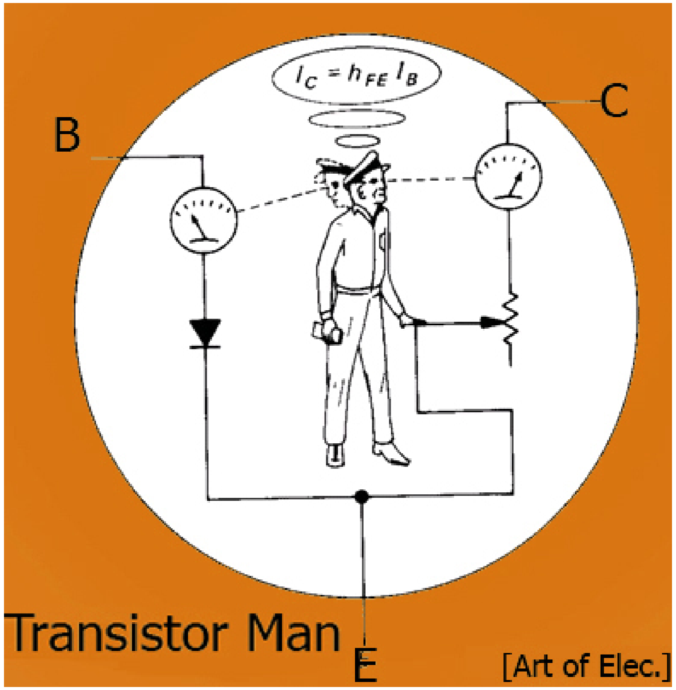

It's time for a
COFFEE
BREAK
www.multimedia.tangentedepi.pt

Refresher: Amplication

Transistors

A classical transistor allows a small current to control a much larger current:





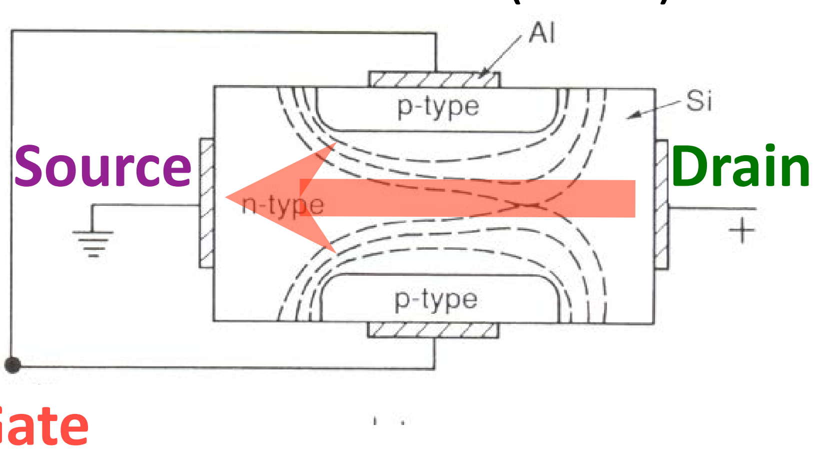
TWO main types of components in IR arrays:

1. Field effect transistors (FETs) - the <u>first stage</u> of amplification
2. Operational Amplifiers (Op Amps) - <u>second</u> and subsequent stages

Field Effect Transistors

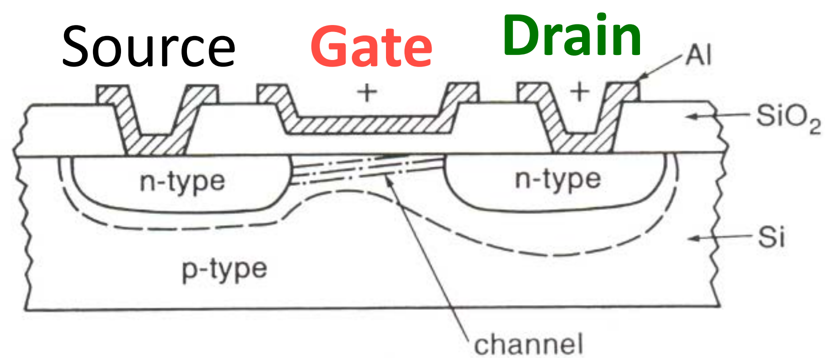
In both types of Field Effect Transistors, the current flows from the SOURCE to the DRAIN controlled by the applied electric field at the GATE

Junction FETs (JFETs)



When depletion regions join, no current flows. Beyond that point, small changes at the gate produce large changes in the drain-source current

Metal-Oxide Semiconductor FETs (MOSFETs)

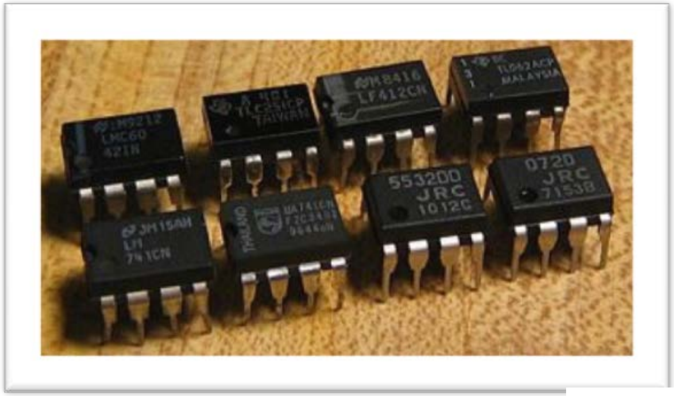


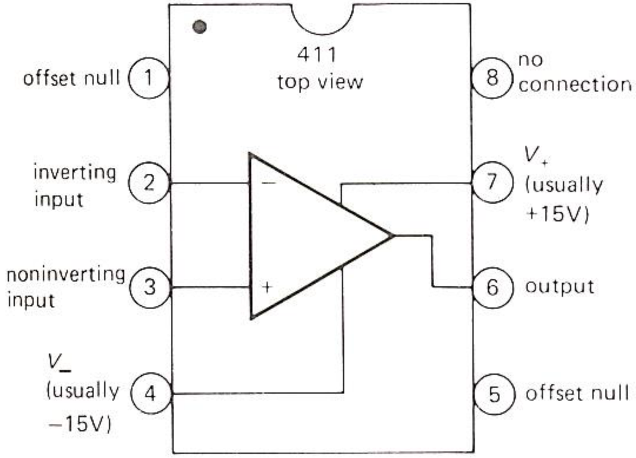
Two n-type dopants implanted into p-type substrate, isolated from each other.

If positive voltage is applied to gate, electrons gather below the insulator and current flows from source to drain

OP Amps

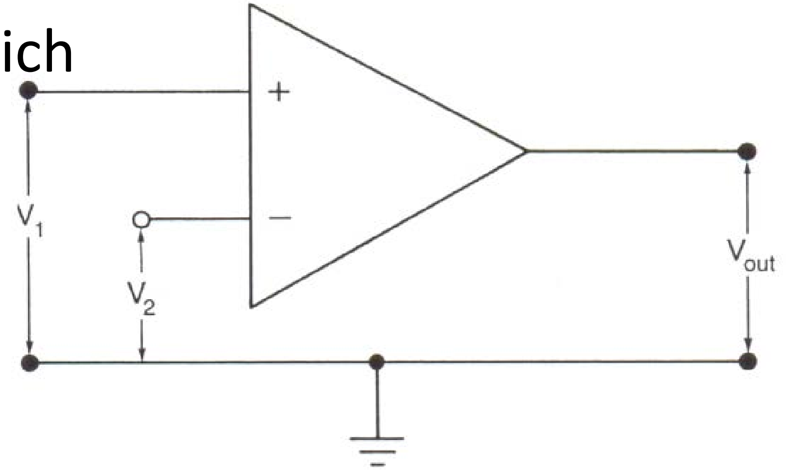
OP Amps are often the second stage of amplification





They are complex integrated circuits which can be understood as a single element:

$$V_{out} \propto |V_1 - V_2|$$



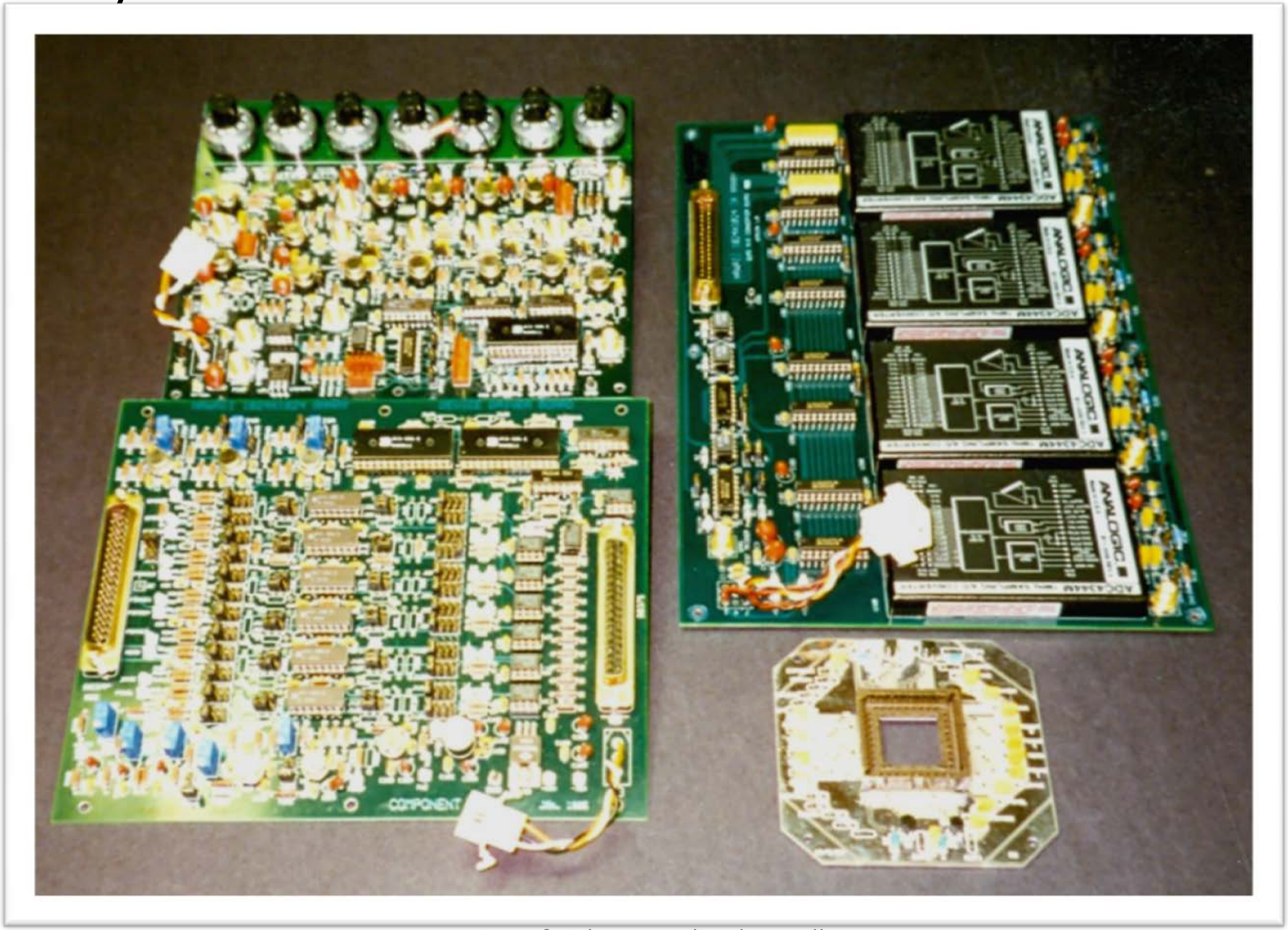
Golden rule I : *The output does whatever is necessary to make the voltage difference between the inputs zero.*

Golden rule II : *The inputs draw no current.*

Infrared Array Readout

Building Blocks of IR Detector Electronics

Example: The *Palomar High Angular Resolution Observer* detector electronics system:



Tasks of a Multiplexer

A multiplexer is needed to address (read or reset) one pixel at a time. “Pixel signals on sequential output lines“ is called multiplexing.

A multiplexer (MUX) has the following functions:

1. Directly address pixels by turning on their amplifiers. (Pixels in other columns with power off will not contribute)
2. Allow for sophisticated readout schemes
3. Allow for subarray reading

A detector with a multiplexer does *not* require moving charges across the array, and one can read out pixels in any order (“random access”)

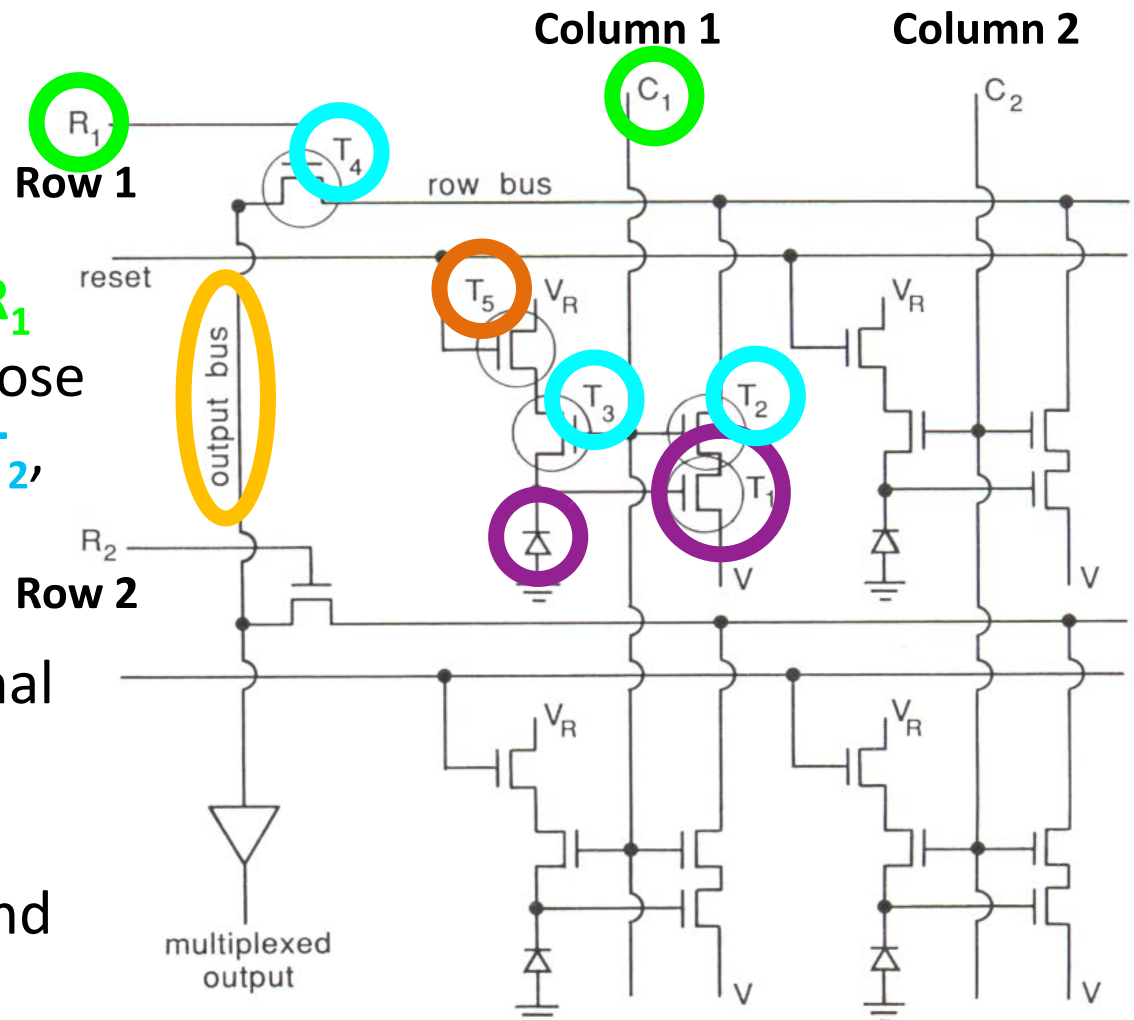
Multiplexer Circuit

Signal at photodiode is measured at gate T_1

Readout uses row driver R_1 and column driver C_1 to close the switching transistors T_2, T_3, T_4.

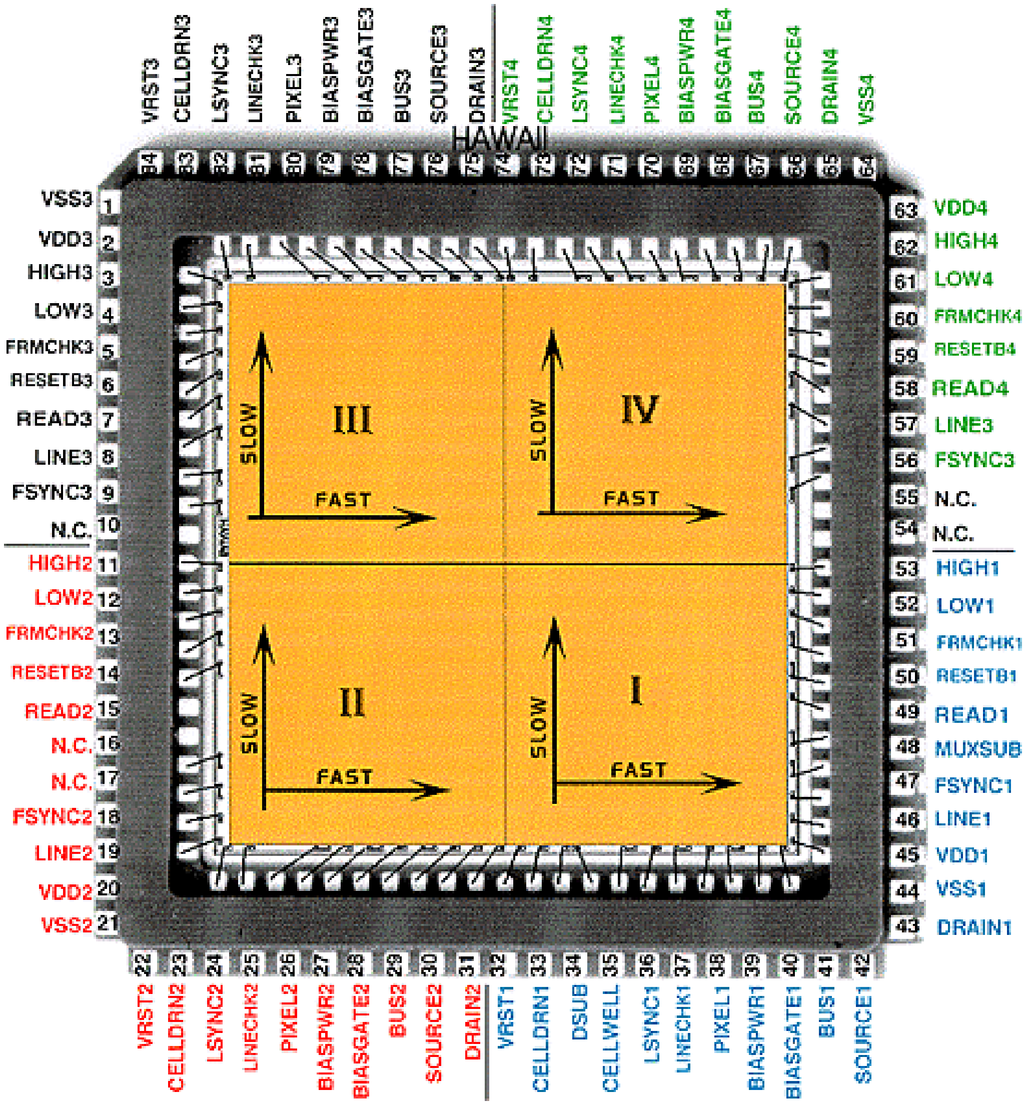
→ Power to T_1 moves signal to the output bus

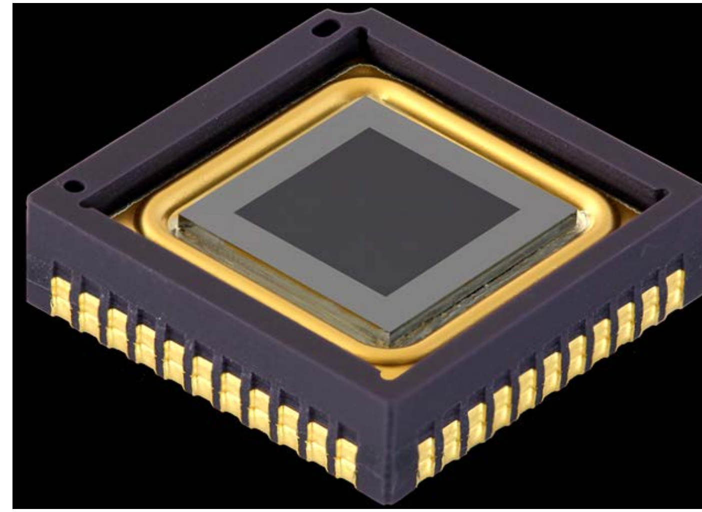
Reset: connect V_R via T_5 and T_3.



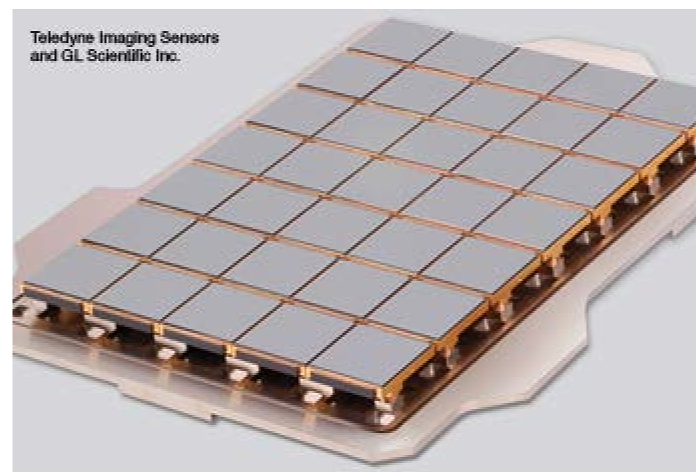
In- and Output Lines

Typical wiring diagram



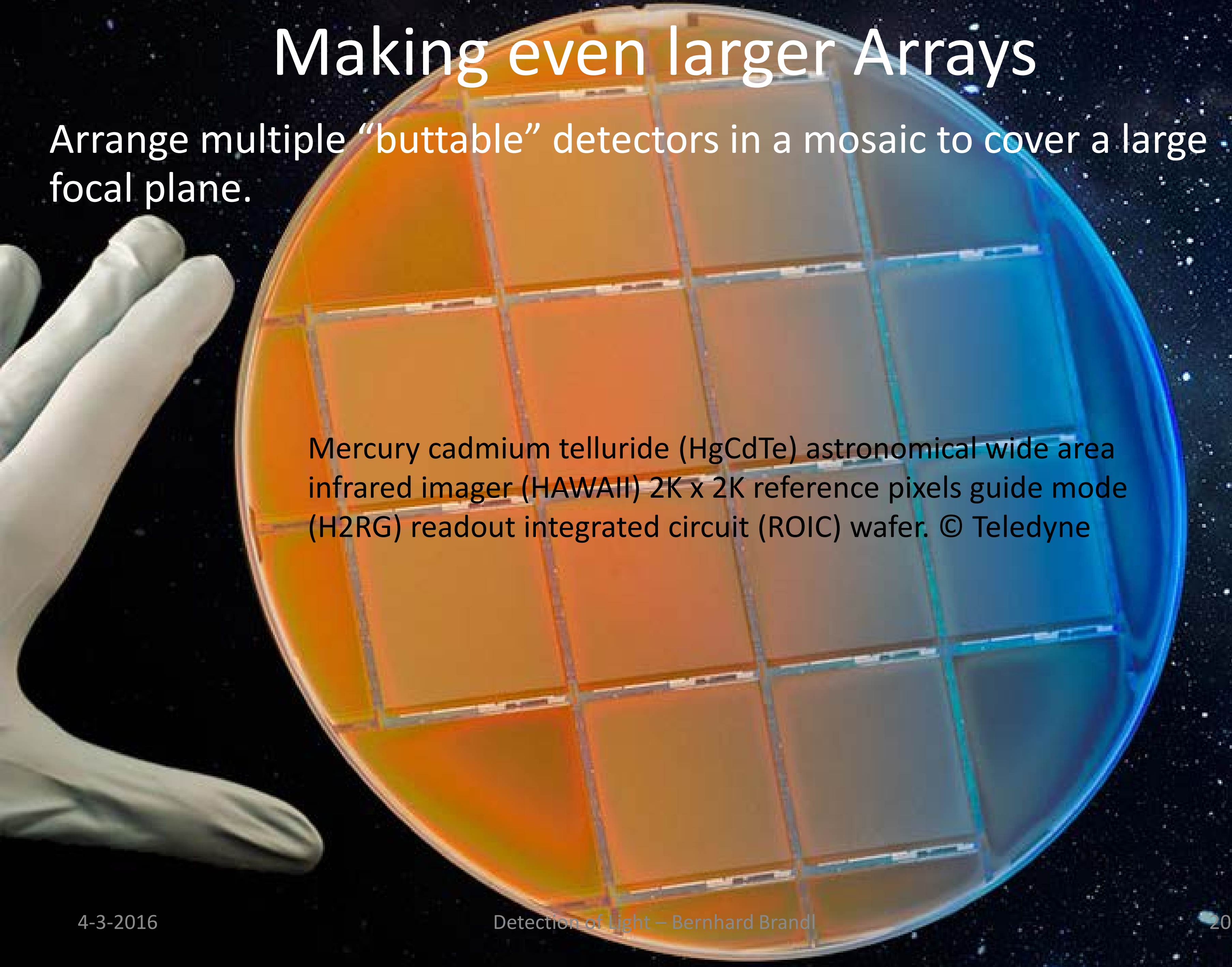


Note that most arrays are not "buttable" since the contacts are at the side → gaps of ~1cm



Making even larger Arrays

Arrange multiple “buttable” detectors in a mosaic to cover a large focal plane.



Mercury cadmium telluride (HgCdTe) astronomical wide area infrared imager (HAWAII) 2K x 2K reference pixels guide mode (H2RG) readout integrated circuit (ROIC) wafer. © Teledyne

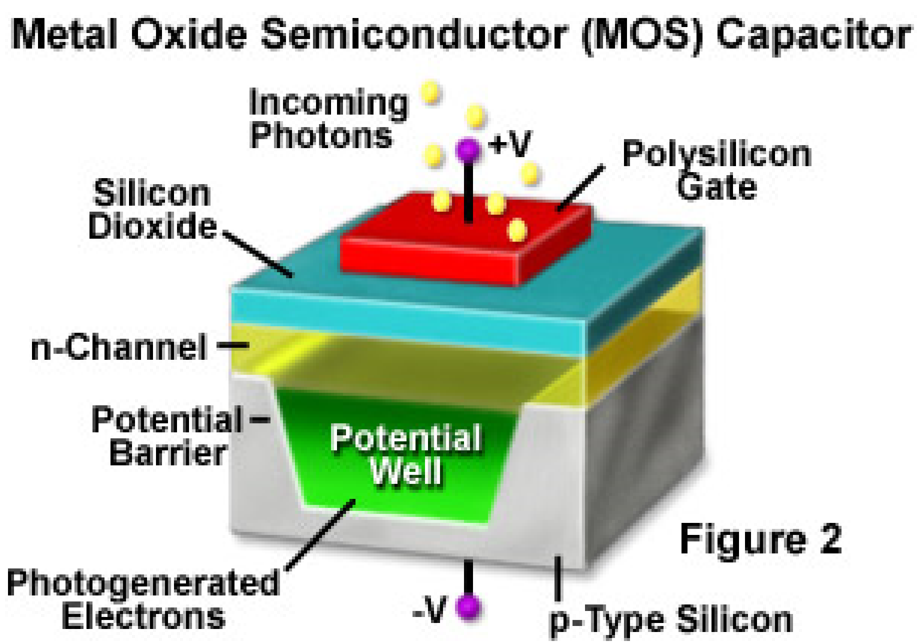
CCDs

(Charge-Coupled Devices)

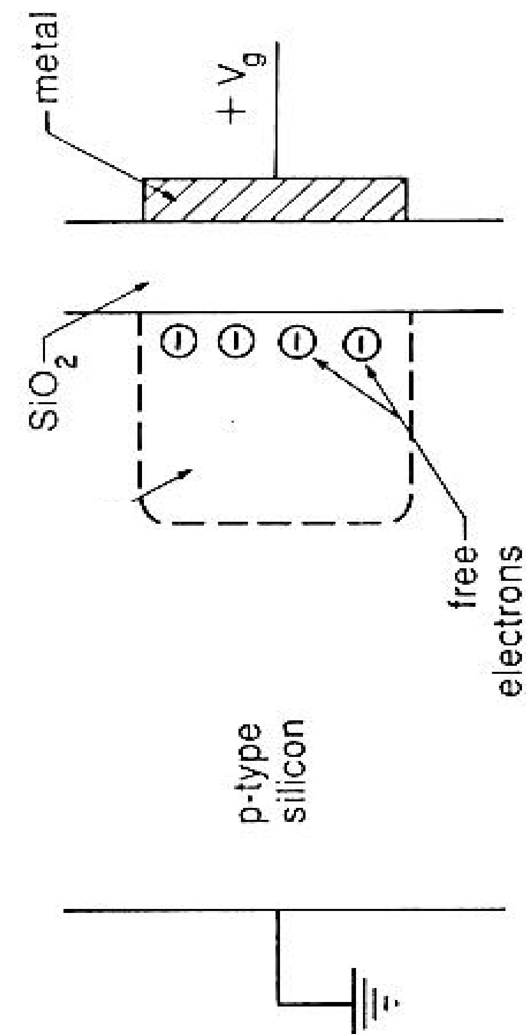
Basic Principle

CCD Pixel Structure

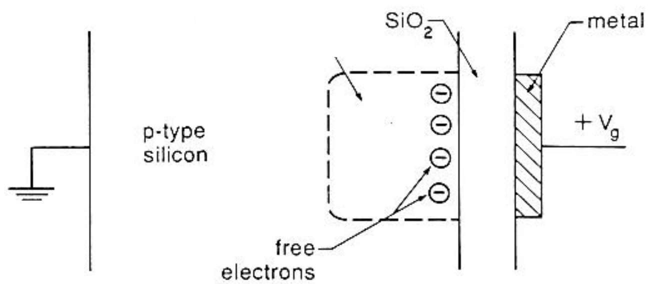
CCD pixels have a metal "gate" evaporated onto SiO_2 (insulator) on silicon ➔ MOS

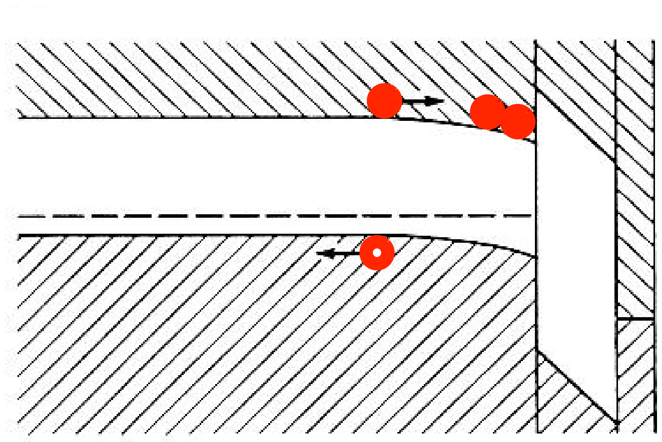


© Hamamatsu

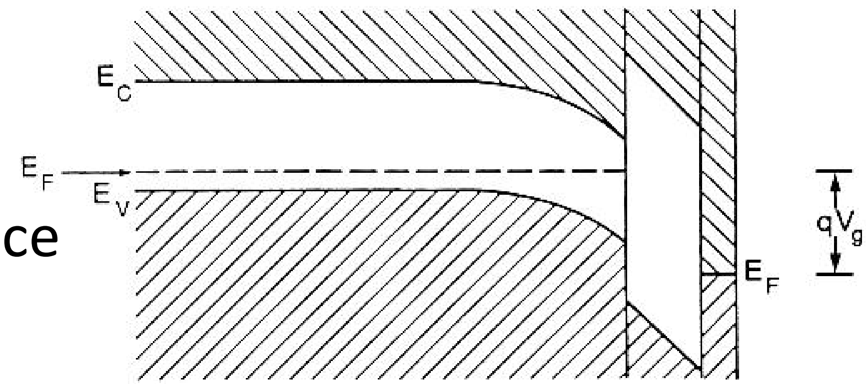


CCD Charge Accumulation

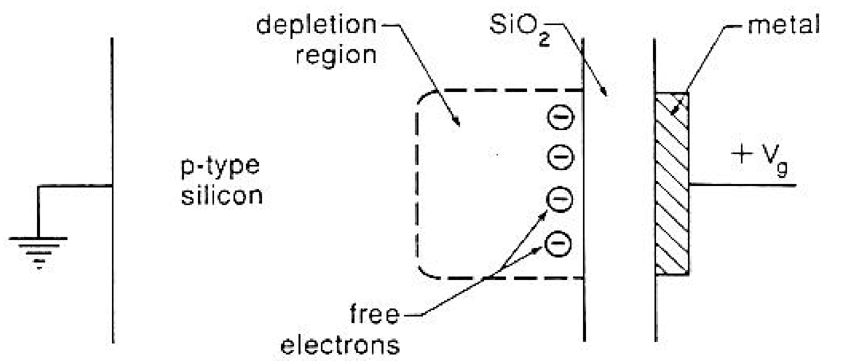




- Photons create free electrons in the photoconductor.
- electrons drift toward the electrode but cannot go through the SiO_2 layer, so they "accumulate" at the SiO_2 interface.
- Total number of electrons at interface is a measure of the number of photons in that pixel during the exposure.

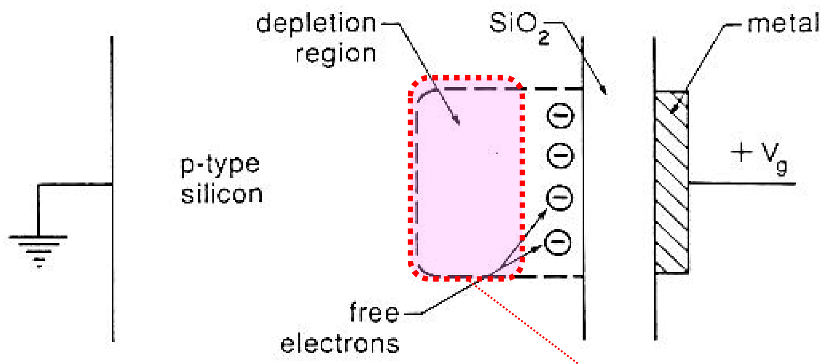


Si Doping and Depletion Region (1)



- In an n-channel CCD, the silicon below the bias gate (+V_g) is slightly *p*-doped.
- The gate is then biased, resulting in the creation of a *n*-channel below the gate and holes are pushed far into the substrate → "deep depletion" (←observers need to "subtract the bias").
- Photon-generated electron–hole pairs in the depletion region are separated by the electric field → electrons move toward the gate, holes toward the substrate.

Si Doping and Depletion Region (2)

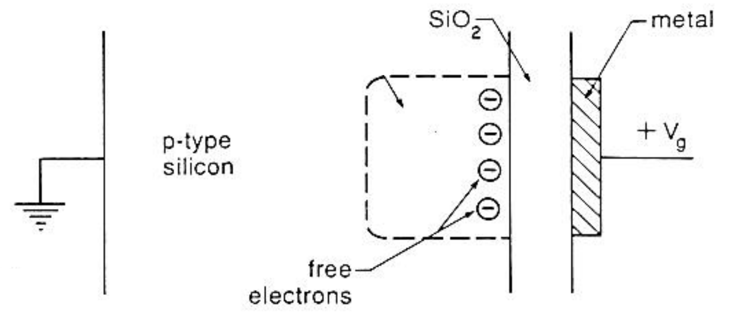


p-type doping leads to the width of depletion region w:

$$w = \left(\frac{2\kappa_0 \varepsilon_0}{q N_D} |V_g| + t_I^2 \right)^{1/2} - t_I$$

where t_I is the thickness of the insulator, N_D the density of ionized donors and κ_0 = 11.8 the dielectric constant of silicon.

Pixel Well Depth



Charges will collect until they balance V_G

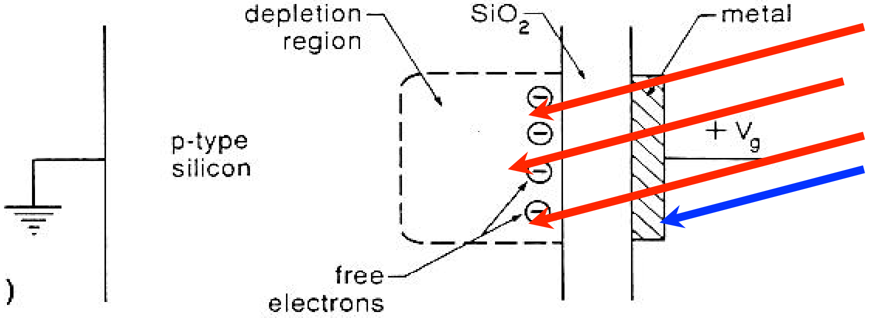
The maximum number of electrons that the MOS capacitor can hold is called the well capacity Q_W:

$$Q_W = C_0(V_g - V_T)$$

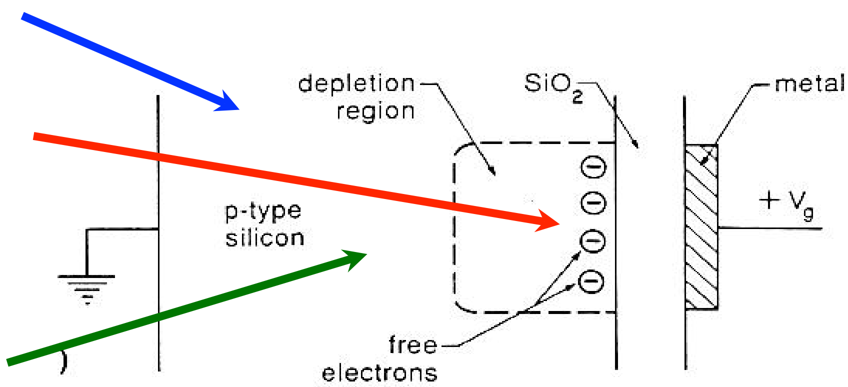
...where V_T is the threshold voltage for the formation of a storage well and C_0 is the pixel capacitance:

$$C_0 = \frac{A\kappa_0\varepsilon_0}{d}$$

Front and Back Illumination



Front illuminated CCDs:
A metal electrode would block incoming photons, so it is made out of heavily doped silicon instead. This leads to problems at blue/UV wavelengths.



Back illuminated CCDs:
UV photons get absorbed near surface of silicon, so there is a lower QE since the photoelectrons need to get trapped in the depletion region.

SOLUTION: mechanically thin the detector so that the UV generated electrons have less distance to travel (*but be careful when you thin...*)

Thinned CCDs

Important considerations for thinning CCDs:

- Thickness must be ≥ one photon absorption length 1/a (if not, photons will be lost)
- a = a(λ), hence the thickness depends on design wavelength [$1/(a_{1\mu m}) = 80\ \mu m$; $1/(a_{0.4\mu m}) = 0.3\ \mu m$!]
- Luckily, the electron diffusion length in low-level doped Si is 10–50 µm [at 150K].
- Good compromise for visible CCDs: thinning to 15–20 µm (at the cost of QE in the red).

> ➢ Making CCDs too thin results in low QE and back reflection from the opposite site (fringing, see below)
>
> ➢ Making CCDs too thick results in wandering into neighbouring depletion zones (loss of spatial resolution)

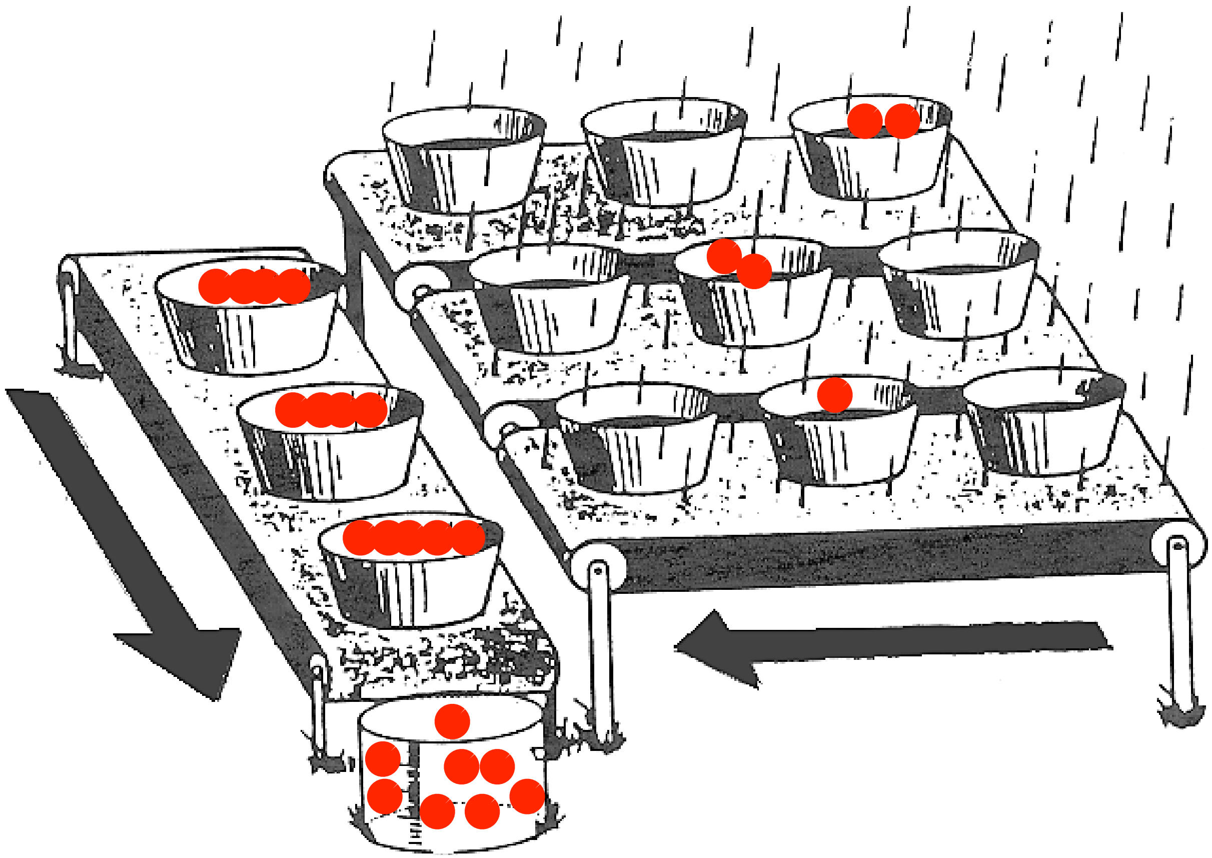
CCDs at wavelengths < 0.3 microns

1. Extremely short photon absorption lengths mean charge collection problems
2. Many “transparent” electrode materials become absorbing
3. Anti-reflection coatings problematic (strong f(λ), and at λ<0.2 μm, n(Si) <1)
4. Specifically developed UV/blue CCDs need a blocking filter for visible light
5. Photons at λ<<0.3 μm generate more than one electron so for X-rays the number of free electrons generated is a measure of the energy of the X-ray photon.

CCDs Readout

CCD Charge Transfer (1)

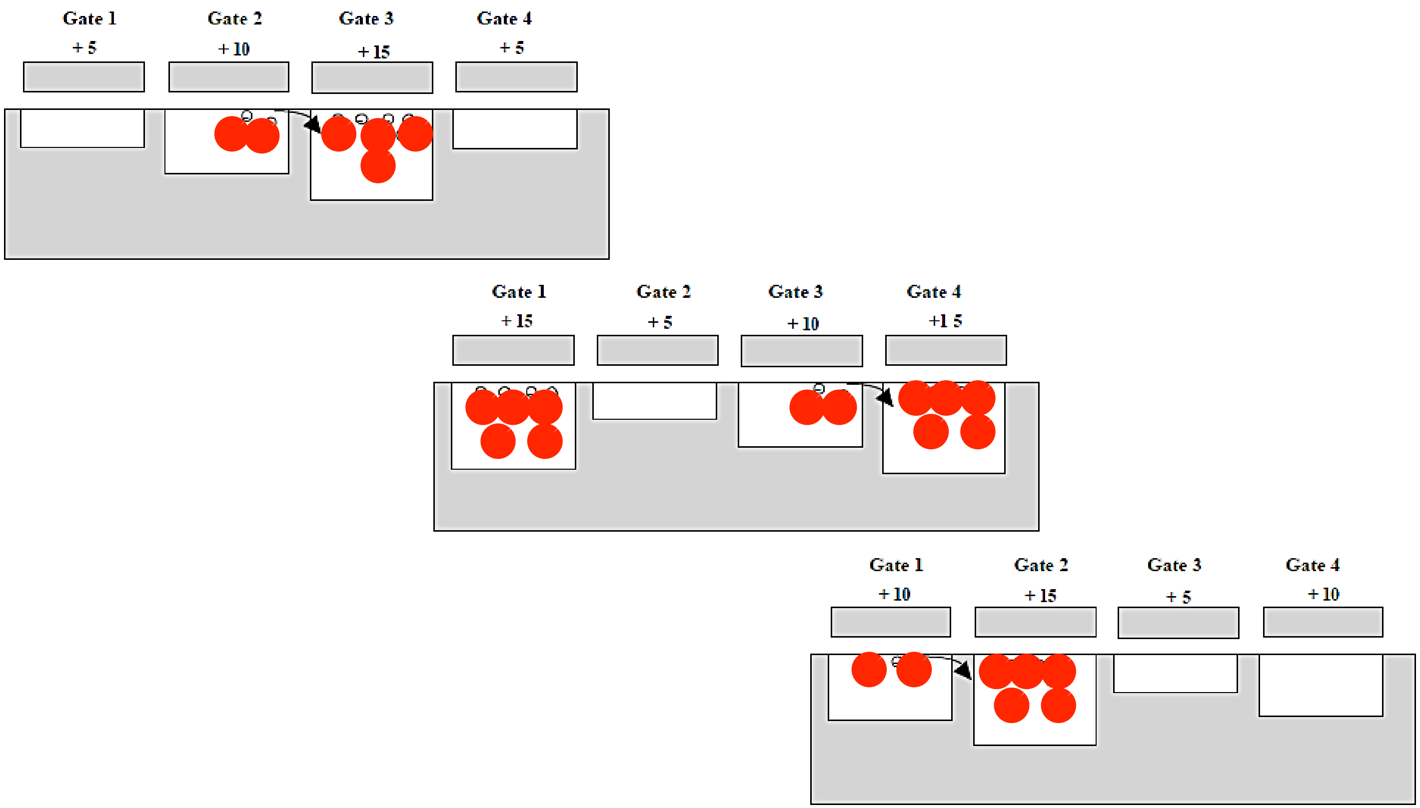
Charges are physically transferred across the array.



The collected charges are passed along the columns to the edge of the array to the output amplifier

CCD Charge Transfer (2)

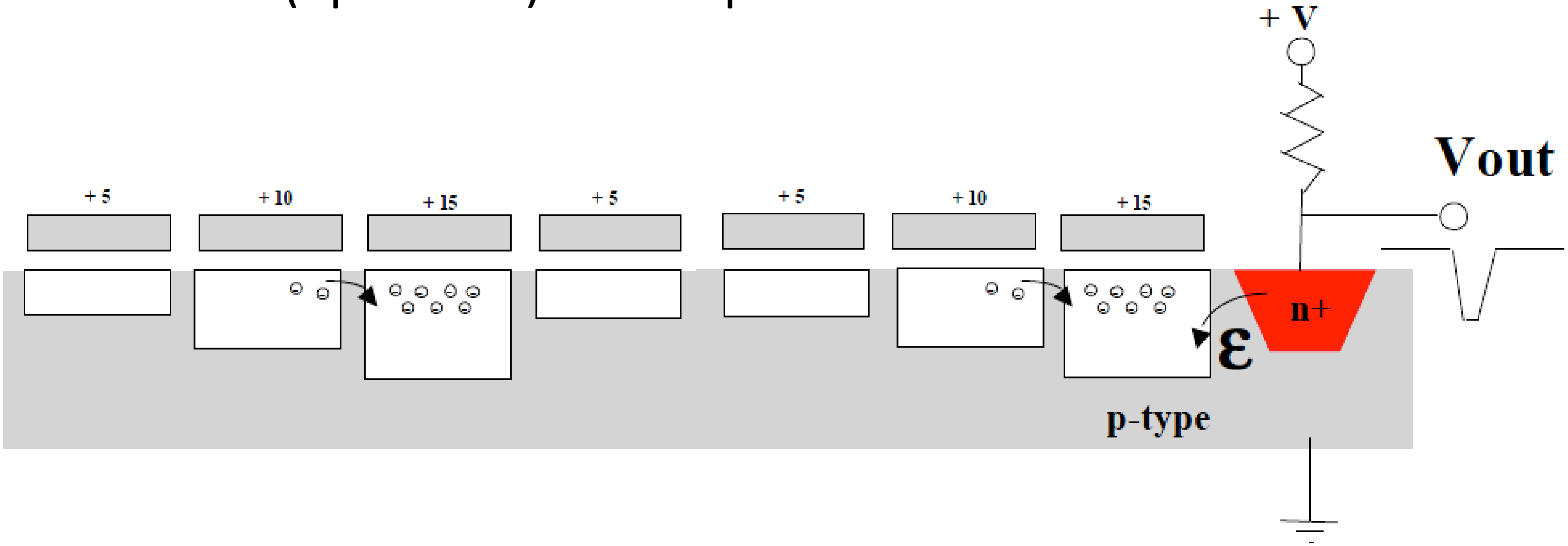
If a potential well is moved together with the surrounding barrier, most of the electric charge will move with it.



Taken from a lecture by Dr. L. Fuller, given at RIT – see http://people.rit.edu/lffeee/lec_CCD.pdf

CCD Charge Transfer (3)

- Eventually, electrons are emptied from the last gate
- the electric field associated with the p-n junction collects electrons that move to +V,
- V_{out} will drop to a level proportional to the number of electrons (~photons) in that packet.

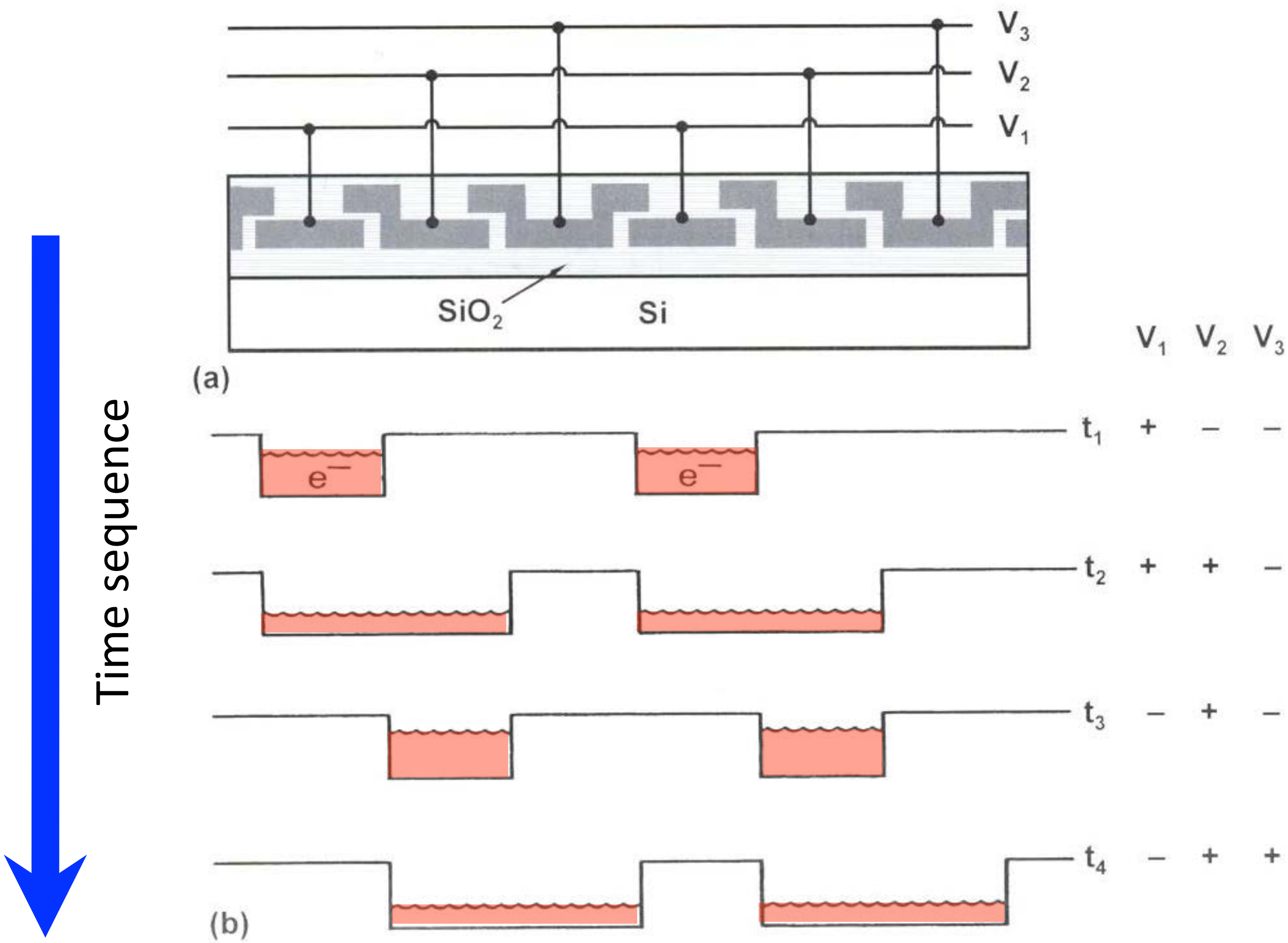


Taken from a lecture by Dr. L. Fuller, given at RIT – see http://people.rit.edu/lffeee/lec_CCD.pdf

2-Phase CCDs

Now, three sets of electrodes laid over each individual pixel.

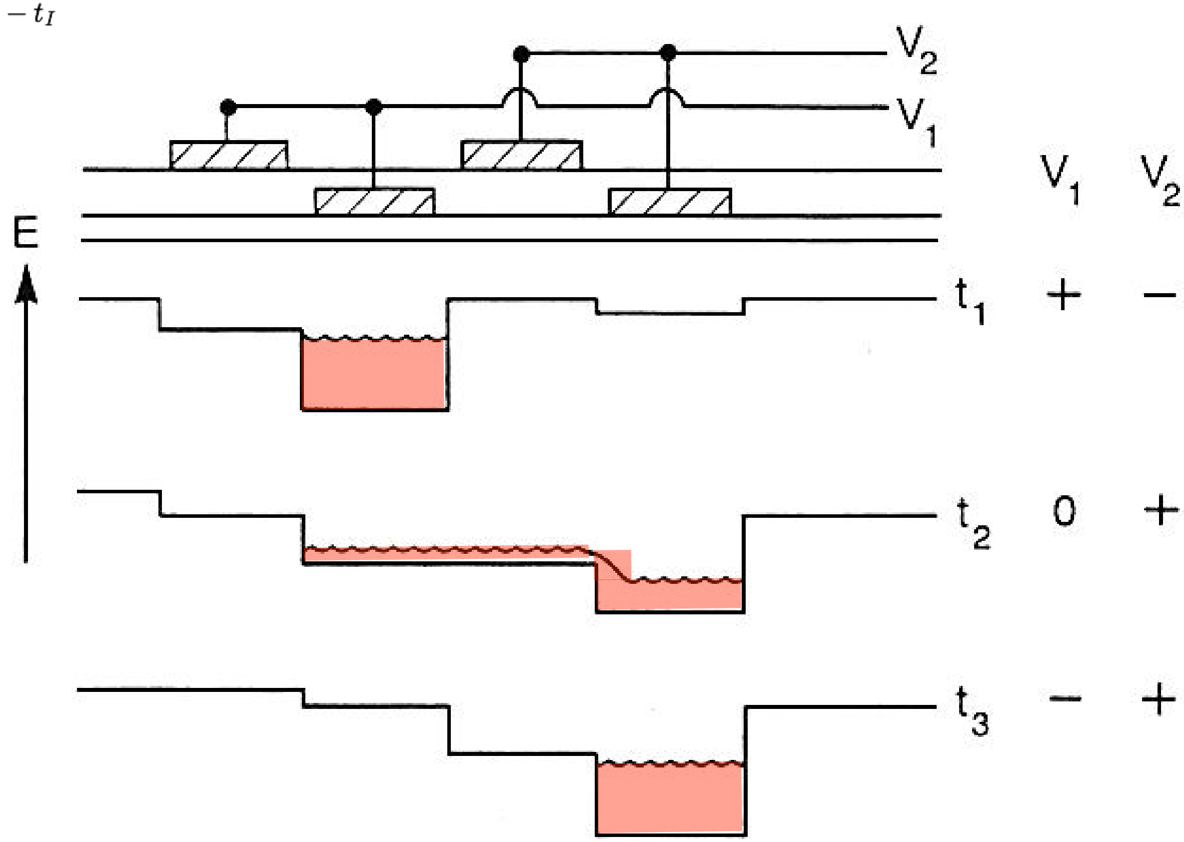
Systematic cycling of voltages between electrodes moves charges.



4 Phase ⇔ 2 Phase Clocking

We can use the dependency of the well depth ω on donor density N_D and insulator thickness t_I to dope in structure in each pixel

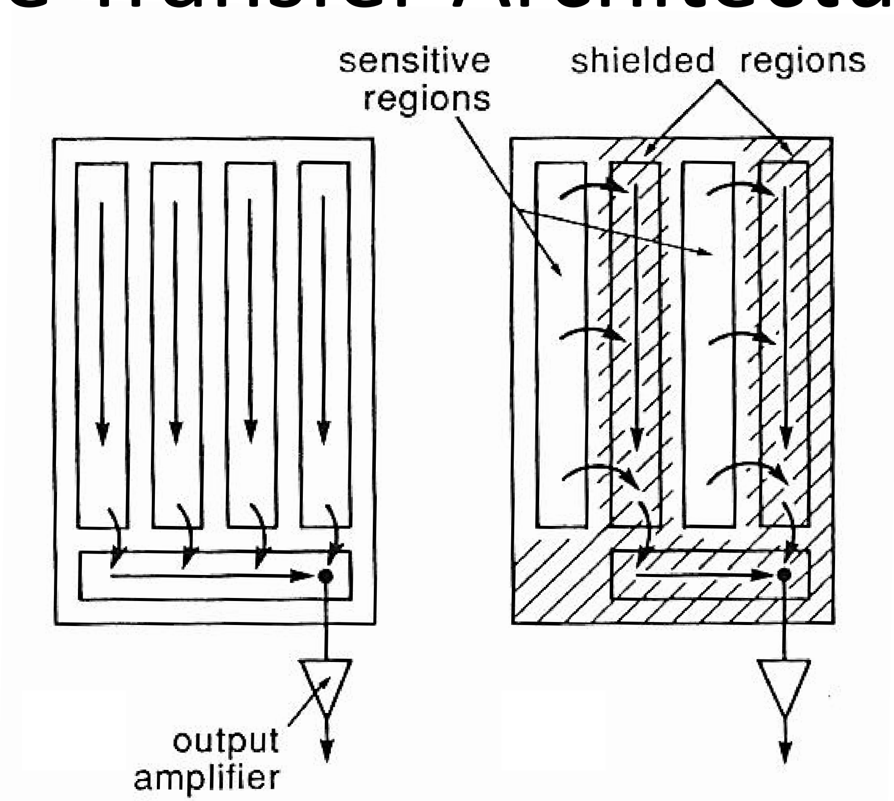
$$w = \left(\frac{2\kappa_0\varepsilon_0}{qN_D}|V_g| + t_I^2\right) - t_I$$



→ we can use a 4 phase CCD as a 2 phase CCD as well

CCD Architecture

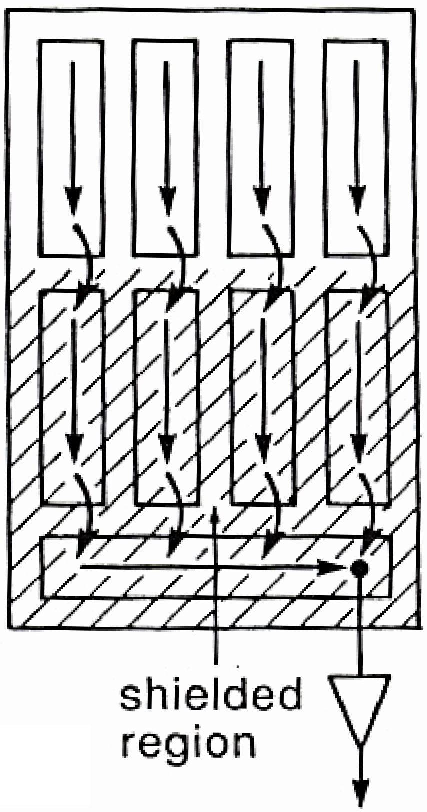
Charge Transfer Architectures (1)

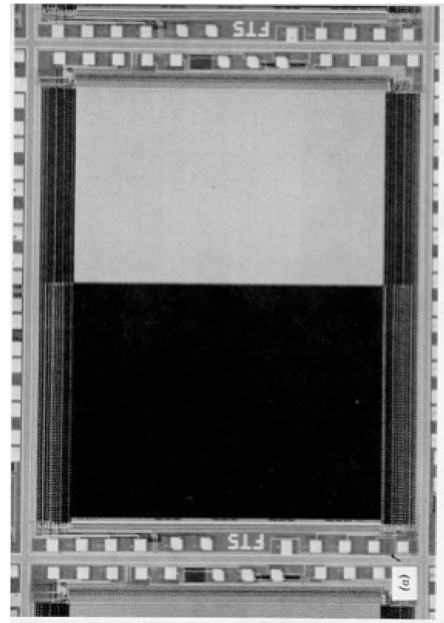


Line address architecture shift contents of columns to output register which then transfers charge to the output amplifier
BUT: array is illuminated whilst the transfers occur ← shutter!

Interline transfer architecture charges are shifted into columns that are shaded from light (the shielded regions)
BUT: low filling factor

Charge Transfer Architectures (2)

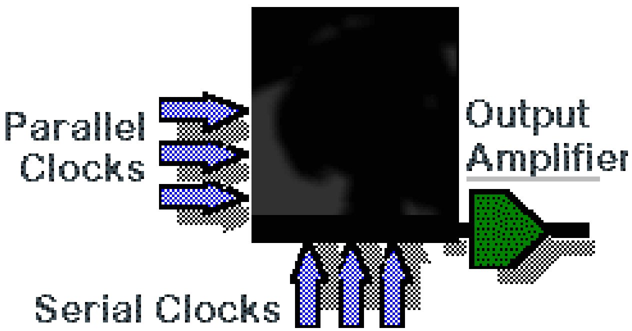




588 lines of 604 pixels, sensor area on top and light shielded storage area at bottom.

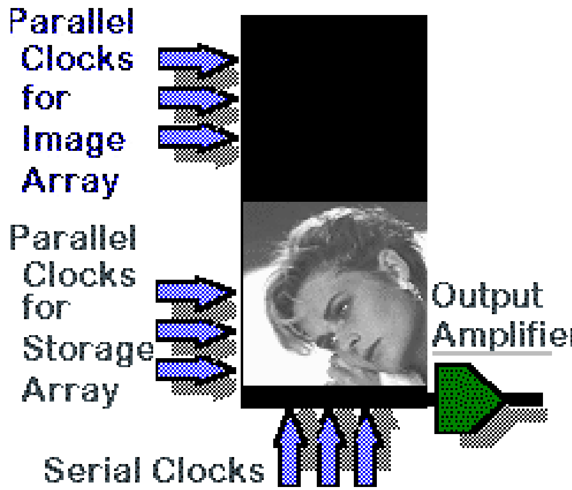
Frame field (frame transfer) architecture charges are rapidly shifted to an adjacent CCD section which is protected from light

Transfer Architectures in Comparison



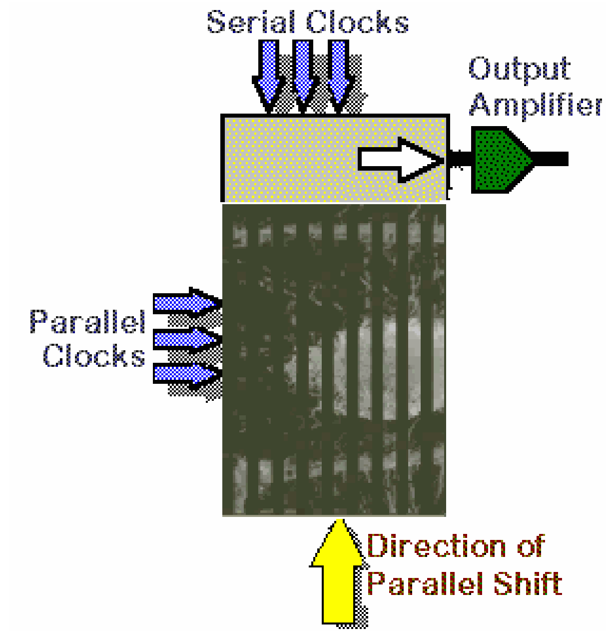
Full frame CCD

- 100% fill factor
- Requires a shutter



Frame transfer CCD

- operates w/o shutter
- requires double size



Interline CCD

- allows very fast R/O
- only 25% fill factor

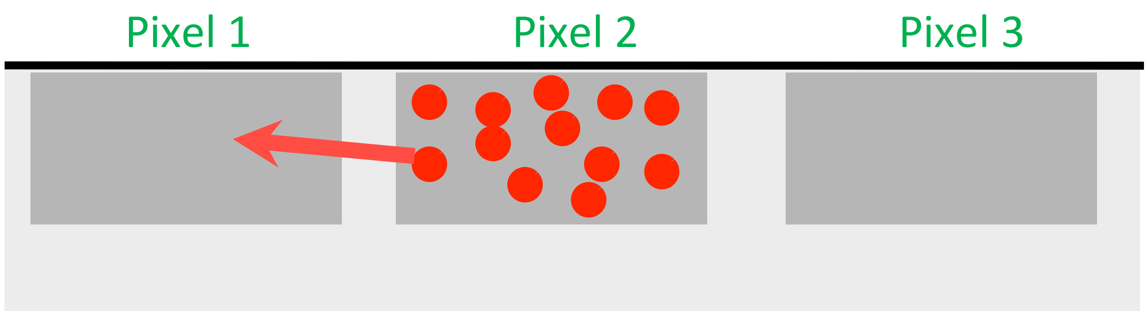
http://www.roper.co.jp/Html/roper/tech_note/html/tarchitectures.htm

CCDs
Charge Transfer Efficiency (CTE)

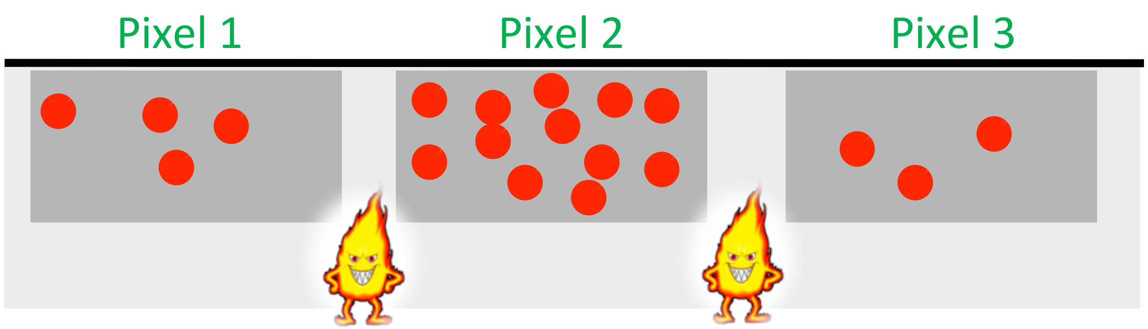
Charge Transfer Efficiency (1)

The CTE is a measure of what fraction of the total number of charge carriers is moved from one pixel to the next.

Problem: A large charge in one pixel will have internal electrostatic repulsion on a characteristic timescale:



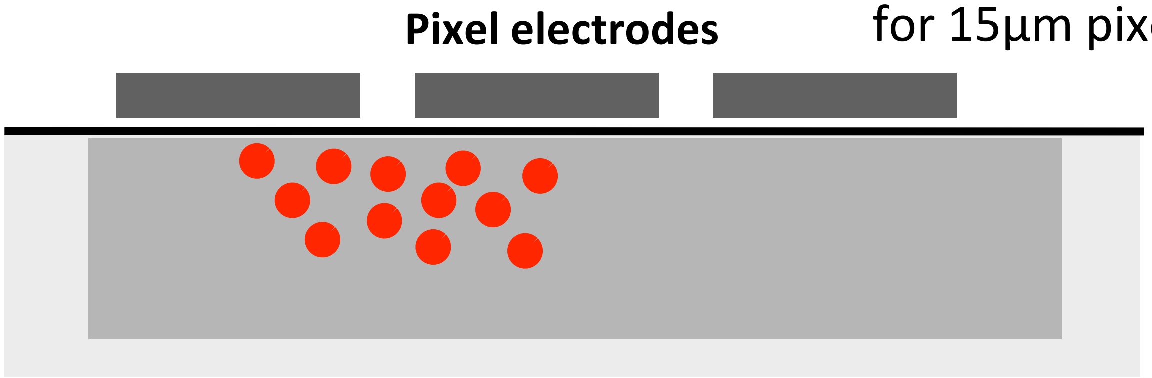
Problem: Thermal diffusion depends on electrode size L_e and diffusion constant D as: $\tau_{TH} \approx \frac{L_e^2}{D}$ (for T=300K, τ_{TH} = 0.026μs)



Charge Transfer Efficiency (2)

Problem: the electric fields near the corners of the electrodes round off corners of pixels ("Fringing fields").

for 15µm pixels, $\tau_{FF} = 0.004\mu s$



For a properly designed CCD with partially filled wells, electrostatic repulsion and fringing fields will dominate.

Approximation for the CTE of a CCD with *m* phases:

$$CTE = (1 - e^{-t/\tau})^m$$

Noise from Charge Transfer

Noise from charge transfer inefficiency: $\varepsilon = (1 - CTE)$

A total of εN_0 charges are "left behind", and the noise on them is $(\varepsilon N_0)^{1/2}$ in each transfer.

In n transfers the net uncertainty is $N_{n,TL} = (2\varepsilon n N_0)^{1/2}$

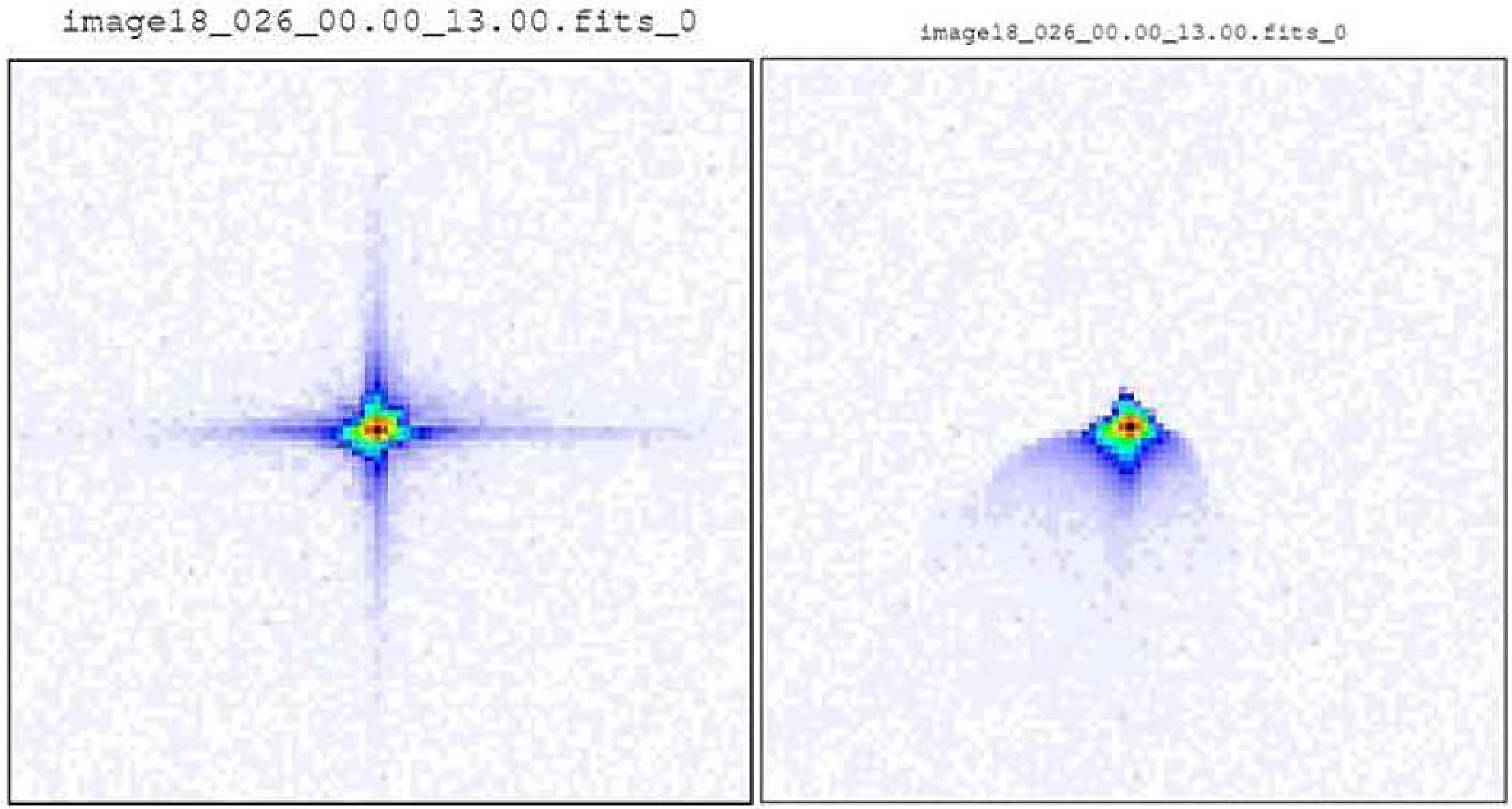
Noise from trapping of charge carriers in incomplete bonds in the Si-SiO_2 interface. Traps will be occupied in equilibrium, but subject to statistical fluctuations with noise

$$N_{n,T} = (2kTnN_{SS}A)^{1/2}$$

(N_{SS} is the density of traps, and A the interface area)

Example: the CCDs aboard GAIA

Cosmic radiation affects the CTE and the point spread function (PSF)



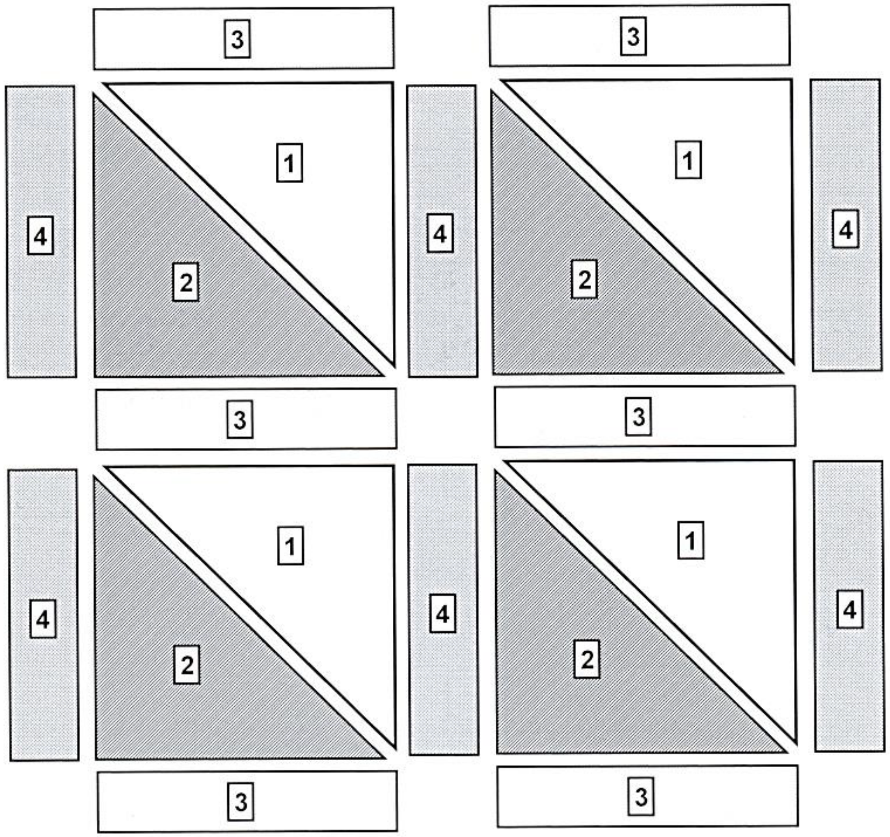
Output from the Gaia CCD model showing the effects of radiation damage. Left: Image of a 13-th mag G2V star before radiation damage. Right: Image of the same star after a 10^{10} proton (10 MeV equivalent) displacement damage dose.

OTCCD, CID & CMOS

Orthogonal Transfer CCDs (OTCCD)

OTCCDs can move charges in two dimensions.

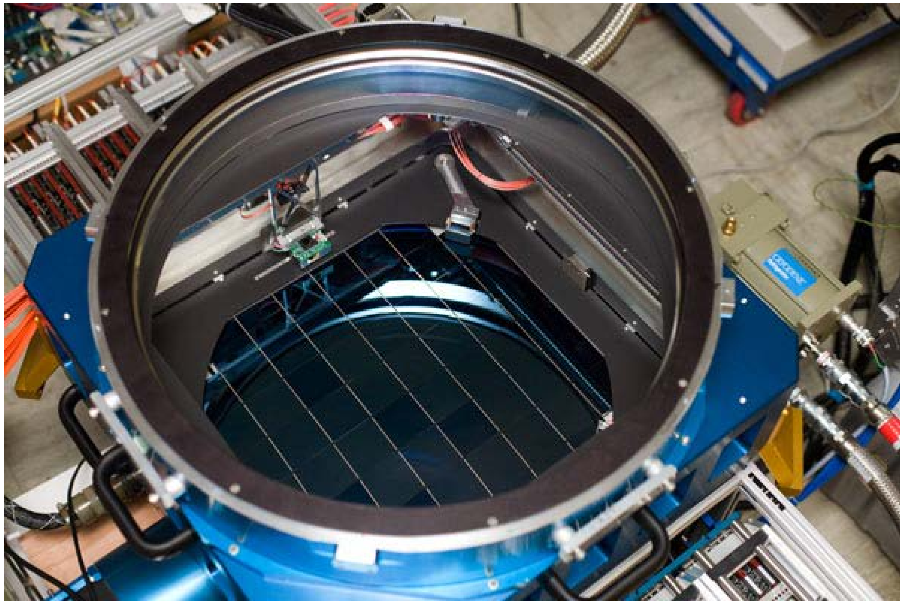
- To move a charge to the right, `3' is negative to act as channel stop, `1', `2', and `4' are operated as a conventional CCD.
- To move a charge up, `4' is negative to act as channel stop, `1', `2', and `3' are operated as a conventional CCD.
- Moving to the opposite directions: reversing the clocking.

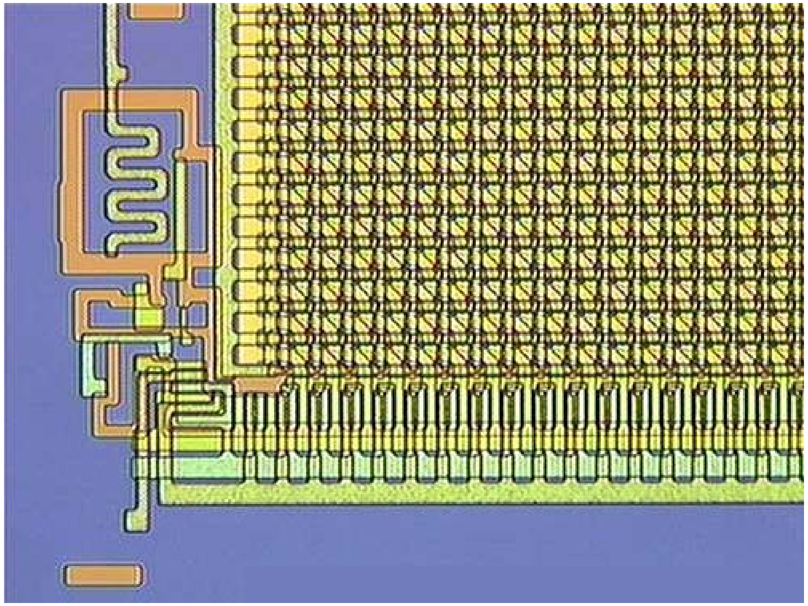


Example: Pan-STARRS (1)

The Panoramic Survey Telescope & Rapid Response System (Pan-STARRS) is a wide-field imaging facility that observes the entire available sky several times each month.

Pan-STARRS combines four 1.8m telescopes with the largest digital cameras ever built. Each camera has a 64 × 64 array of CCD devices, each containing approximately 600 × 600 pixels, for a total of about 1.4 Gpix.

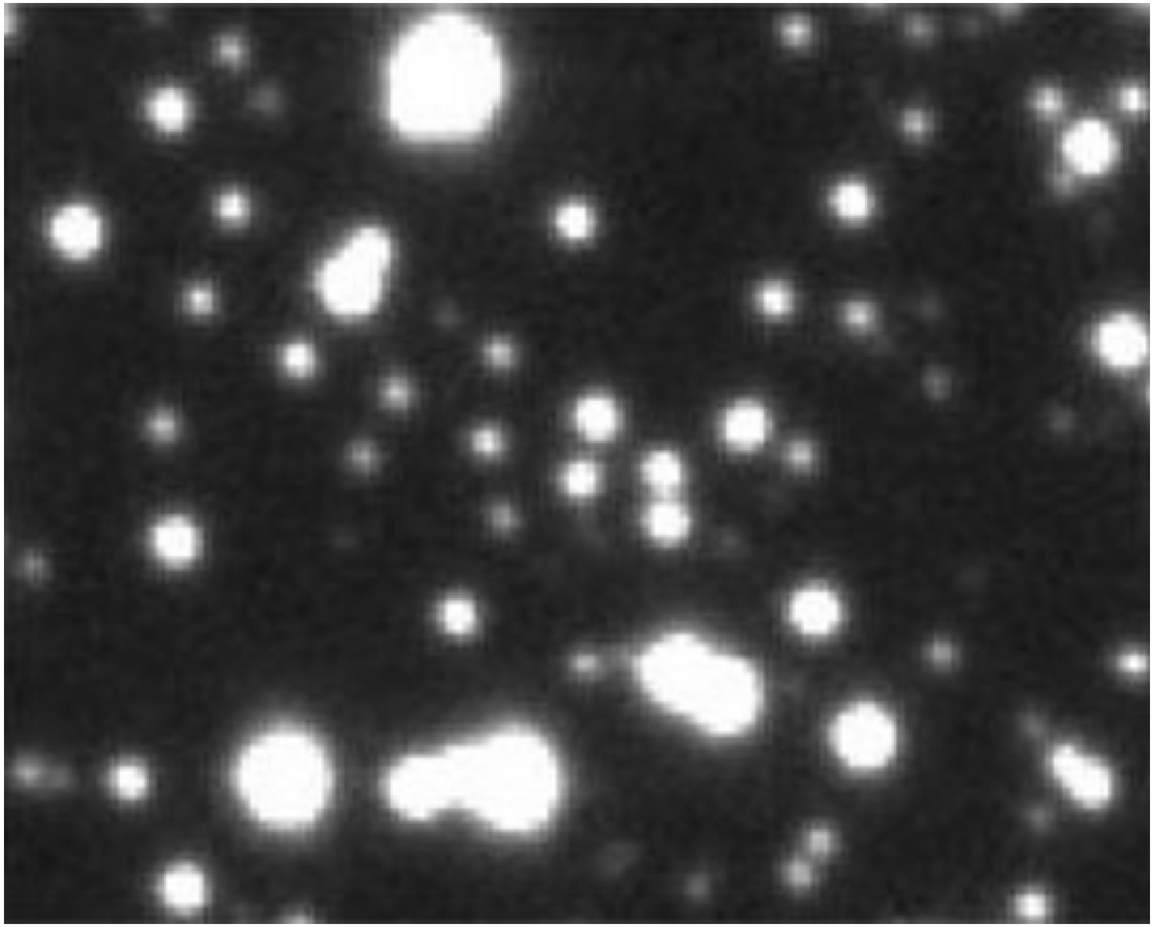




Key-element is a Orthogonal Transfer Charge Coupled Device (OTCCD).

Example: Pan-STARRS (2)

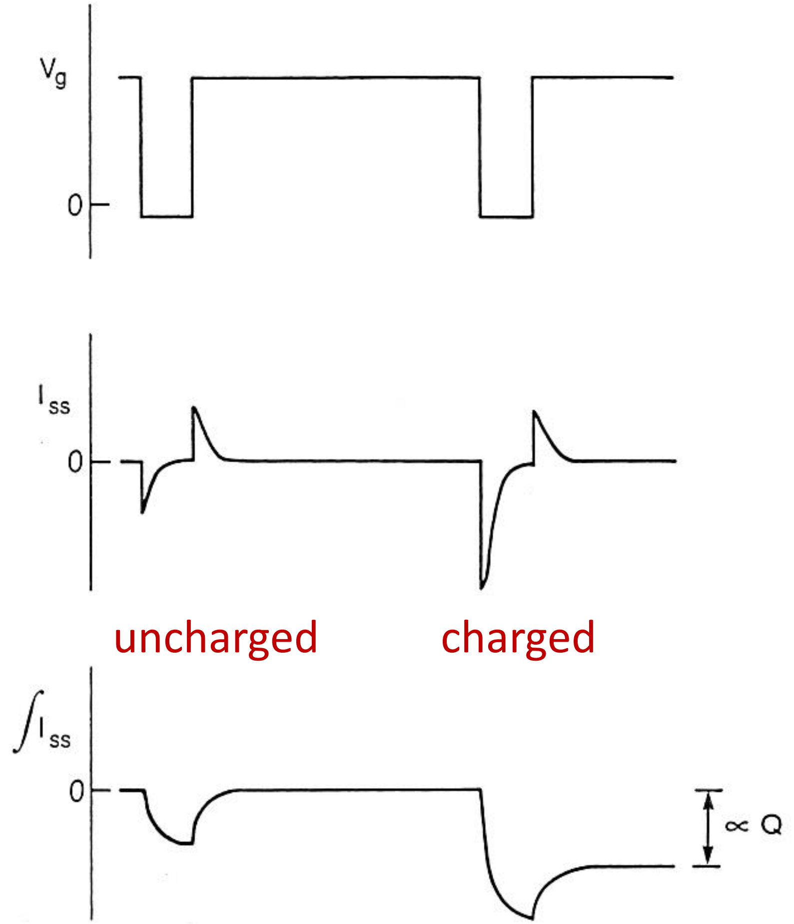
If we can follow the motion of the star on the array, we can compensate for atmospheric tip tilt motion, i.e., improve resolution and sensitivity (analogous to a classical "tip-tilt" mirror system).



Charge Injection Devices (CIDs) (1)

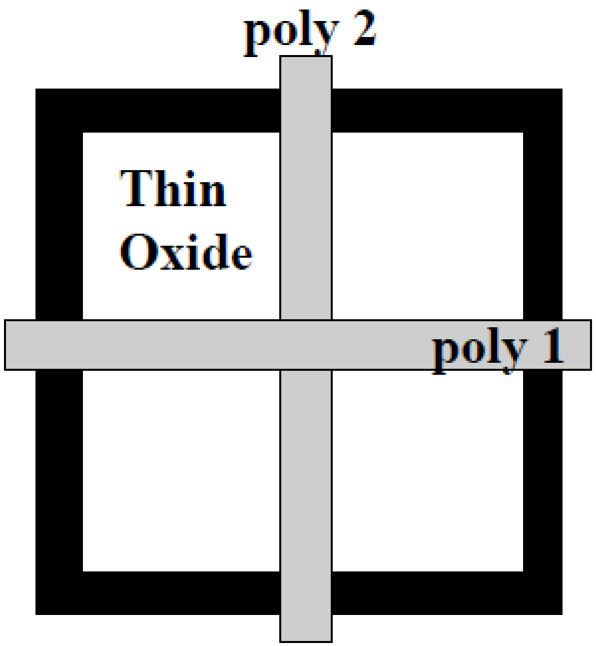
Principle: two electrodes within one pixel "slosh" electrons from one side to the other, acting as a capacitor - apply an electric pulse to the capacitor.

- if uncharged the response will be symmetric and the integral over the current will be zero
- if charged the waveform will be asymmetric: asymmetry ∝ charge
- measure integral over I_{SS}



Charge Injection Devices (CIDs) (2)

Each pixel consists of a pair of MOS capacitors. The two capacitors run perpendicularly to each other and are known as collection and sense pads.



Pros and cons of CIDs:

+ non-destructive reads possible

+ robust in low radiation environments

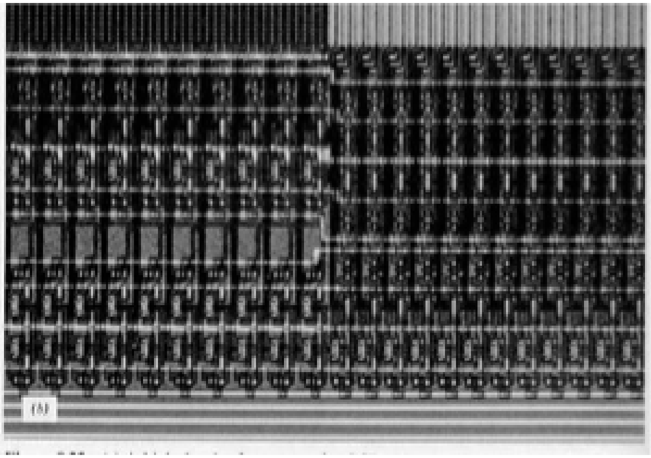
+ large fill factor and good pixel uniformity

– large read noise because an entire row of MOS capacitors is connected at one time.

http://www.photonics.com/EDU/Handbook.aspx?AID=25130
http://www.photonics.com/Article.aspx?AID=52489

Complementary Metal-Oxide-Semiconductors (CMOS)

Nowadays, transistors are tiny and high performance arrays can be manufactured in complementary CMOS devices = Si photodiodes + R/O circuitry on a single Si wafer (analogous to hybrid arrays but in one unit)



Pros and cons of CMOS:

+ much less sensitive to radiation damage

+ allow simplified systems design

– only 70 – 80% fill factor

– ~50 e^- read noise

Fill factor may be increased with micro-lens arrays

Colour CCDs

Essentially three ways to produce color (from Wikipedia) :

1. Take three exposures through three filters subsequently – standard for astronomy (only works for fixed targets).
2. Split the input beam in three channels, each with a separate and optimized CCD (very expensive cameras).
3. Use a Bayer mask over the CCD – each subset of 4 pixels has one filtered red, one blue, and two green (reduced fill factor).